COUNTER-BASED CLOCK DOUBLER CIRCUITS AND METHODS WITH OPTIONAL DUTY CYCLE CORRECTION AND OFFSET

ABSTRACT

Clock doubler circuits and methods use counters to define the positions of the output clock edges. A plurality of counters are each clocked by a count clock relatively much faster than the input clock. A first counter counts for one input clock period, and the counted value is stored. The stored value is divided by two to provide the number of counts in half of the input clock period. The divided value is provided to a second counter that counts from zero to the divided value. Thus, the second counter generates a pulse halfway through the input clock period. Other counters running at the same clock rate can be used to generate pulses at other times in the input clock cycle, as desired. The pulses from the counters are used in combination with the input clock signal to provide output clock edges at predetermined times during the input clock cycle.